Description

JMT N-channel Enhancement Mode Power MOSFET

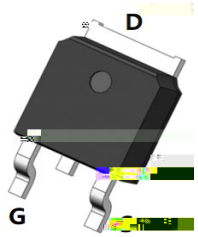
Features

Lead Free

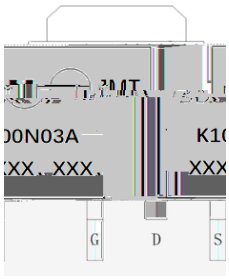
Applications

- Load Switch
- PWM Application
- Power Management

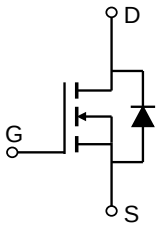
100% UIS TESTED!
100% ûVds TESTED!



TO-252-3L(DPAK) Top View



Marking and Pin Assignment



Schematic Diagram

Electrical Characteristics (T_J = 25℃ unless otherwise specified)

Symbol	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics					
$V_{(BR)DSS}$		30	-	-	V
I_{DSS}		-	-	1.0	μA
I_{GSS}		-	-	–100	nA
$V_{GS(th)}$		1.2	1.6	2.2	V
		-	7.8	10.0	mΩ
		-	11.5	15.0	mΩ
C_{iss}		-			
		-			
		C			

Test Circuit

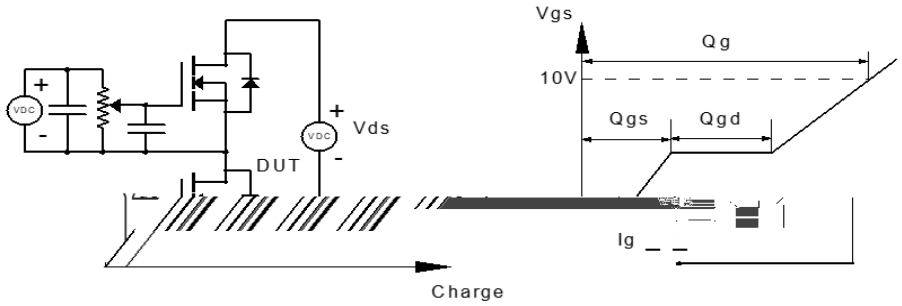


Figure 1: Gate Charge Test Circuit & Waveform

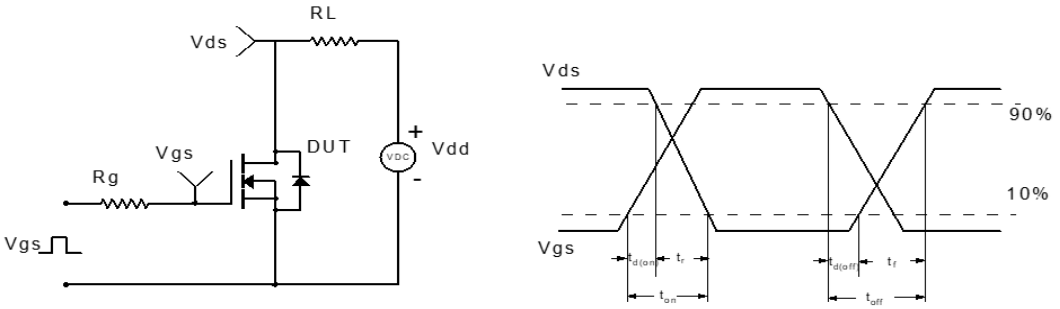


Figure 2: Resistive Switching Test Circuit & Waveform

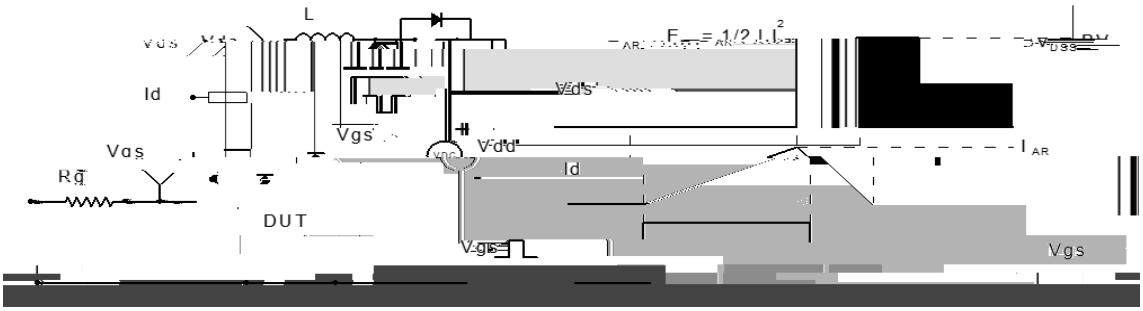


Figure 3: Unclamped Inductive Switching Test Circuit& Waveform

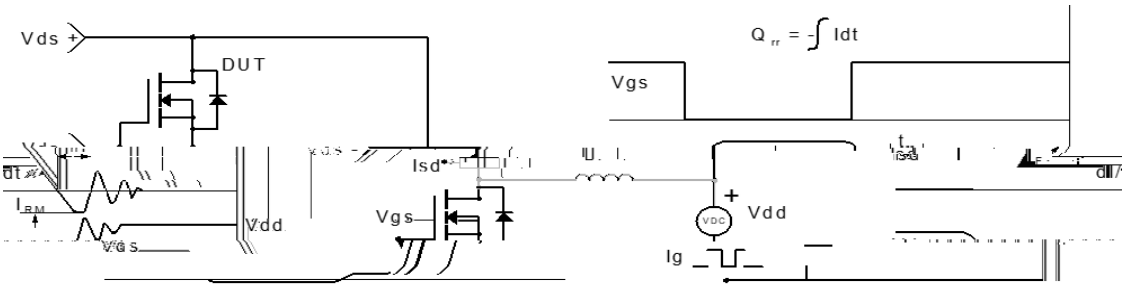
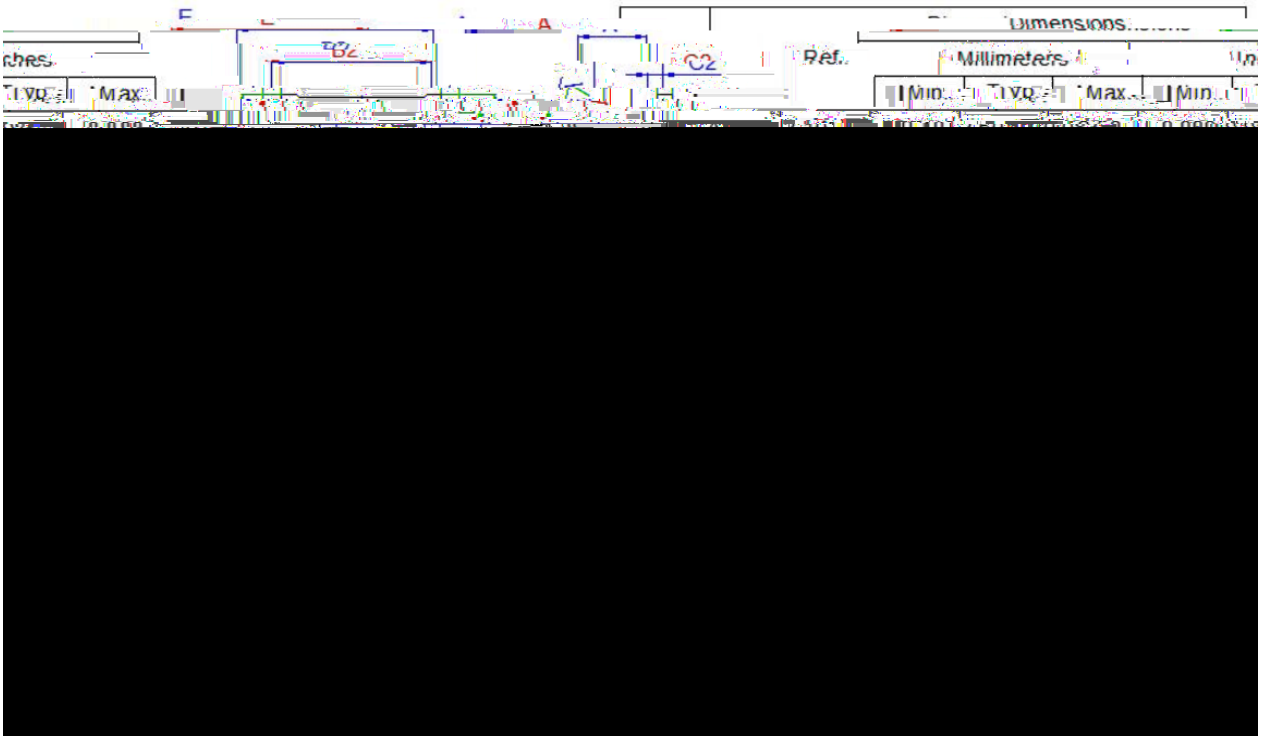


Figure 4: Diode Recovery Test Circuit & Waveform

Package Mechanical Data(TO-252-3L)



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